Introduction to SoC
(System-on-a Chip)
Chip Everywhere!
Wafer & Die & Packaging

Assembly/Packaging

Wafer

Die
SoC Industry

- **SoC design** (cp. 建築設計師)
  - 聯發科
- **SoC process technology** (cp. 營造廠)
  - 台積電、聯電
- **SoC package and testing** (cp. 裝潢)
  - 日月光
- **SoC CAD** (電腦自動化)
Integrated Circuits (ICs)
IC Design History

- **In 1970’s (Small, Medium-Scaled IC, or SSI, MSI)**
  - The layout was the design
  - IC design was an ART
  - No simulation, no verification

- **In 1980’s (Large, Very-Scaled IC, or LSI, VLSI)**
  - Technology CMOS 2.0~1.0
  - Design complexity 30K~400K transistors
  - Daisy, DEC (2MB RAM, .5GB HD, 1MIPS)
  - Logic simulation, Verification, CAD layout
  - ASICs

- **In 1990’s (Ultra Large-Scaled IC, ULSI)**
  - Technology CMOS 1.0~0.18
  - Design complexity 400K~10M gates
  - SUN Sparc, Pentium4 (4GB-16GB, 1 Terabyte HD)
  - Synthesis, P&R
  - ASICs, Processors, Embedded software, FPGA

- **In 2000’s (System-on-a-Chip or SoC)**
# Evolution of Microelectronics (1)

<table>
<thead>
<tr>
<th>ERA</th>
<th>Date</th>
<th>Complexity</th>
<th>Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Transistor</td>
<td>1959</td>
<td>Less than 1</td>
<td></td>
</tr>
<tr>
<td>Unit Logic (one gate)</td>
<td>1960</td>
<td>1</td>
<td>diode</td>
</tr>
<tr>
<td>Multi - Function</td>
<td>1962</td>
<td>2 - 4</td>
<td>logic gates, FF</td>
</tr>
<tr>
<td>Complex Function</td>
<td>1964</td>
<td>5 - 20</td>
<td>counter, adder multipliers</td>
</tr>
<tr>
<td>MSI</td>
<td>1967</td>
<td>2 - 200</td>
<td>8-bit up, RAM</td>
</tr>
<tr>
<td>LSI</td>
<td>1972</td>
<td>200 - 2000</td>
<td>16 &amp; 32 bits up peripherals</td>
</tr>
<tr>
<td>VLSI</td>
<td>1978</td>
<td>2000 - 20000</td>
<td>special and real time processor</td>
</tr>
<tr>
<td>ULSI</td>
<td>1989</td>
<td>20000 - ?</td>
<td>?</td>
</tr>
</tbody>
</table>
Evolution of Microelectronics (2)

- Today’s Silicon process technology
  - 0.13μm CMOS
  - ~100 M of devices, 3GHz internal clock
- Yesterday’s chips are today’s function blocks
MOS (Metal Oxide Semiconductor)
Changes in Real IC

Source: L.-R. Zheng, KTH

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.8μm</th>
<th>0.18μm</th>
<th>0.07μm</th>
</tr>
</thead>
<tbody>
<tr>
<td># of Metal layers</td>
<td>2~3</td>
<td>6</td>
<td>8-9</td>
</tr>
<tr>
<td>G.W. Aspect ratio (t/w):</td>
<td>~0.8</td>
<td>~1.8</td>
<td>~2.7</td>
</tr>
<tr>
<td>Wire length (m/chip):</td>
<td>~130</td>
<td>~1,480</td>
<td>~10,000</td>
</tr>
</tbody>
</table>

Interconnects Start to Dominates Cost and Performance
Interconnect starts to be main design constraints

Source: L.-R. Zheng, KTH
Layout and chip microphotograph
Moore’s Law and Technology Scaling

“…the performance of an IC, including the number of components on it, doubles every 18-24 months with the chip price…” –Gordon Moore 1960
Moore’s Law in Action

Example:

Intel Pentium 4 microprocessor evolution

- 0.18 micro technology
  - 42M transistors
  - Die size: 217 mm²

- 0.13 micro technology
  - 55M transistors
  - Die size: 146 mm²

Source: Intel
製程技術演進與預測

矽的故事

Gate Length


10000 1000 100 10 1

Transistor Number per chip

10^{15} 10^{14} 10^{13} 10^{12} 10^{11} 10^{10} 10^{9} 10^{8} 10^{7} 10^{6}

DRAM
1.4 Times/Year

Neuron Number in Brain

Increasing Technology difficulty

64GB (2015) 1TB (2023)
### Expectation By SRC Roadmap

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum feature of size (mm)</td>
<td>0.35</td>
<td>0.25</td>
<td>0.18</td>
<td>0.13</td>
<td>0.10</td>
<td>0.07</td>
</tr>
<tr>
<td>Memory in bits/chip (DRAM/FLASH)</td>
<td>64M</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
</tr>
<tr>
<td>Microprocessor transistor per chip (2.3 times per generation)</td>
<td>12M</td>
<td>28M</td>
<td>64M</td>
<td>150M</td>
<td>350M</td>
<td>800M</td>
</tr>
<tr>
<td>ASIC (gate per chip)</td>
<td>5M</td>
<td>14M</td>
<td>26M</td>
<td>50M</td>
<td>210M</td>
<td>430M</td>
</tr>
<tr>
<td>Chip frequency (MHz) for a high-performance on-chip clock</td>
<td>300</td>
<td>450</td>
<td>600</td>
<td>800</td>
<td>1,000</td>
<td>1,100</td>
</tr>
<tr>
<td>Maximum number of wiring levels (logic), on chip</td>
<td>4-5</td>
<td>5</td>
<td>5-6</td>
<td>6</td>
<td>6-7</td>
<td>7-8</td>
</tr>
<tr>
<td>Power supply voltage (V) for desktop</td>
<td>3.3</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>0.9</td>
</tr>
<tr>
<td>Maximum power for high performance with heat sink (W)</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>140</td>
<td>160</td>
<td>180</td>
</tr>
</tbody>
</table>

Source: SIA (Semiconductor Industry Association) road map
VLSI Applications

- Microprocessors or microcontroller
  - Pentium, ARM, DSP processors

- Memory
  - DRAM, SRAM, ROM, ..

- Special purpose processors
  - Audio, image or video compression
    - Image: JPEG, JPEG2000
    - Video: MPEG1,2,4,7, H.26x
    - Audio: MP3, AC3,
  - Communication (wired or wireless)

- Information Appliance (IA)
System Development Flow

Applications

Specifications

System Design

Component Design

Marketing

Testing

Fabrication

Placement & Routing

Layout

Synthesis

Hardware: CPU, RAM, I/O...

Software: C, C++

always @(posedge clk)
begin
if (sel1) begin
out = in1;
else
out = in2;
end
end

1.8 吋 TFT

其他

傳輸距離：100 m
功能：影像傳輸、語音傳輸
螢幕：176 x 220 pixel
65535 色
IC Industry Segments in Taiwan

- Integrated Device Manufacturers (IDM)
- Foundries
- Fabless Semiconductor Companies
- EDA Vendors
## IC Designers

<table>
<thead>
<tr>
<th>Who</th>
<th>What to do</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Design Engineer</td>
<td>Specification Definition</td>
</tr>
<tr>
<td>ASIC Design Engineer</td>
<td>Behavioral Design and Simulation</td>
</tr>
<tr>
<td>IP Design Engineer</td>
<td>Register Transfer Level (RTL) Design, Simulation and Testing</td>
</tr>
<tr>
<td>Circuit Design Engineer</td>
<td>Gate/Switch/Circuit Level Design, Simulation and Testing</td>
</tr>
<tr>
<td>CAD Engineer</td>
<td></td>
</tr>
<tr>
<td>Test Engineer</td>
<td></td>
</tr>
<tr>
<td>IC Layout Engineer</td>
<td>Physical Layout</td>
</tr>
<tr>
<td></td>
<td>Layout Verification</td>
</tr>
<tr>
<td></td>
<td>Post-layout Verification (Simulation)</td>
</tr>
</tbody>
</table>
Remark: Silicon Pendulum

- **standardization**
  - flexibility
  - time to market
  - cost effectiveness

- **customization**
  - performance
  - differentiation
  - value addition

![Diagram showing the relationship between ASIC, Configurable Hardware, and Programmable Processors on a performance and flexibility axis.](image-url)
SoC: System on Chip?

- System
  A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.

- A SoC design is a “product creation process” which
  - Starts at identifying the end-user needs (or system)
    - Hardware
    - Software
  - Ends at delivering a product with enough functional satisfaction to overcome the payment from the end-user
SoC Evolution

First phase

second phase

third phase

- Logic
- ROM
- SRAM
- uP Core
- ROM
- PLL
- AD DA
- Soft I/F Core
- uP Core
- ROM
- Flash
- DSP Core
- SRAM
- DRAM
- Application Specific IP Core
- PLL
- Application Specific Analog
- AD DA
- Logic
- Soft I/F Core
- Logic
- Analog
- DRAM
- Flash
What is SoC in your mind?

**Definition:** integration of a complete system onto a single IC
SoC Architecture

- Memory
- Processor
  - Embedded Software
  - RTOS
- DSP or Special FU
- OCB Architecture
- Configurable Hardware
- RF
- Mixed Signal
- J TAG
- Interface
- Peripherals
SOC is industry trend

- **Today**
  - Assembly
  - SOC

- **Tomorrow**
  - Integration
  - IP/System-Board

- **Current**
  - ASIC/ASSP
  - System-Board
SoC Applications

Source: Semico Research Corp.
Example: Mobile Phone

Yesterday

- Voice only; 2 processors
- 4 year product life cycle
- Short talk time

Today

Single Chip
- 5~8 Processors
- Memory
- Graphics
- Bluetooth
- GPS
- Radio
- WLAN

- Voice, data, video, SMS
- <12 month product life cycle
- Lower power; longer talk time

Source: EI-SONICS
Why SoC?

**Why?**
- Complex applications
  - Semiconductor density ↑ 58% per year, but design productivity ↑ 21% annually.
- Process technology allows it
- High performance
- Miniaturization
- Battery life
- Short market windows
- Cost sensitivity

**Characteristics**
- Very large transistor counts on a single IC
- Mixed technologies on the same chip
  - Digital, memory, analog, FPGA
  - Hardware and software
- Multiple clock frequencies
- Hierarchical design with embedded reusable IP cores
Benefits of Using SoC

- Reduce overall system cost
- Increase performance
- Lower power consumption
- Reduce size
Traditional vs. Core-Based IC Design

- **Traditional IC Design**
  - Design IC from scratch
  - Reuse: standard-cell library, memories, local ‘Copy & Change’

- **Core-Based IC Design**
  - Reuse of large modules: cores, IP, megacells, system-level macros, virtual components
  - Examples: CPU, DSP, MPEG, JPEG, communication modules, memories, analog modules
  - Reduced time-to-market, expertise import
Where SoC Goes To?
SoC and SIP

- **System-on-Chip (SoC)**
- **Semiconductor Intellectual Property (IP)**
  - Also known as cores, virtual components (VCs)
  - Memory, processors, DSPs, I/O, peripherials

- SoC = $\sum$ IPs?
Why IP?

- Don’t know how to do it
- Cannot wait for new in-house development
- Standard/Compatibility calls for it
  - PCI, USB, IEEE1394, Bluetooth
  - Software compatibility
- Configurable
A platform is a suite of reusable parts (IP) of many system designs in a limited spectrum of applications.

Source: SOC Design Overview /MOE, R.O.C.
Platform Example

Wipro’s ARM-based SoC-RapTor Platform
Benefits of Using SoC

- Reduce overall system cost
- Increase performance
- Lower power consumption
- Reduce size
SoC - New Design Era

New design consideration

– Design methodology
  • Platform-based design

– Functionality implementation
  • Personal reuse
  • In-house reuse
  • IP reuse
  • Architecture reuse

Reuse without redesign

– Multi-level design descriptions

– Physical design consideration/constraint
The New System Design Paradigm

Orthogonalization of concerns: the separation
of function and architecture,
of communication and computation
SoC Design Flow

Specification

High Level Algorithm Model
C/C++/COSSAP/VCC/MATLAB

Hardware/Software Partition
N2C/VCC

Communication Refinement
N2C/Port-C/VCC

Front End

Back End

Chip

Hardware/Software Coverification
N2C/Seamless/"Q/Bridge"

RTOS
WinCE/VxWorks

Device Driver
Driveway

API

Embedded
Software